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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,366	09/19/2000	Douglas O. Powell	EN9-99-026	5058

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EXAMINER	
COMPTON, ERIC B	
ART UNIT	PAPER NUMBER
3726	

DATE MAILED: 09/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/665,366	POWELL, DOUGLAS O.	
	Examiner	Art Unit	
	Eric B. Compton	3726	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-78 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-78 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 1, line 18 is objected to because of the following informalities: --and—(first occurrence) should read –an--. Appropriate correction is required.

2. Claim 67, line 10, is objected to because of the following informalities: --lease— should read –least--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 6-7, requires "forming at least one passage through the dielectric later to expose the layer of electrically conducting material." However, based on the limitation of lines 4-5, the dielectric layer is covered on both its top and bottom surface with an electrically conducting material, and therefore the conducting material is already exposed.

It appears that Applicant wishes to claim providing a hole through one layer of the conducting material as well as the dielectric material, but not through the other layer

of conducting material (as shown in Figure 4). Applicant will need to resolve the claim limitation as such. Claims 2-46 depend from claim 1 and therefore are also indefinite.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-3, 4-10, 12-21, 23-26, 28-33, 36, 42, 45-48, 50- 56, and 63-68, are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 4,915,983 to Lake et al.

Regarding claims 1, 46, and 68, Lake et al disclose a multi-layered electronic structure and a method for making said structure (see Figure 8), comprising the steps of:

a. providing a layer of dielectric material (50) having a top and bottom;

b. providing a layer of electrically conducting material (52,54) on one of the top surface and the bottom surface of the dielectric layer;

c. forming at least one passage (58) through the dielectric layer;

d. depositing electrically conducting material (60) in at least one of the at least one passage through the dielectric layer;

e. removing portions of the layer of electrically conducting material to define a pattern of circuitry (52',54' step 4);

f. stacking a plurality of structures (step 6) comprising the layer of dielectric material and layer of electrically conducting material;

g. aligning the plurality of structures (step 6, it is inherent that the structures are aligned);

h. joining the plurality of structures such that the electrically conducting material in at least one on the at least one passage through the dielectric material electrically connects the conductive pattern disposed on the dielectric layer with another conductive pattern on an adjacent structure of the stacked plurality of structures (by bonding, col 8, lines 62-65); and

i. filling the spaces between the structures with electrically insulating material (via bonding with a thermoset plastic or adhesive, col 9, lines 10-26).

Regarding claims 66 and 67, a electronic package, formed by the method above is shown and described. Furthermore, it is noted that such structure are used for mounting electrical components (col 1, lines 24-27).

Regarding claims 2-3, 5, 47, 48, and 50, Lake et al disclose that the dielectric (50) may be polyimide (col 9, line 33) and/or include a mesh or screen of glass (col 10, lines 37-38).

Regarding claim 6, see Figure 8, step 1 of Lake et al.

Regarding claim 7, Lake et al disclose that the conducting material may be soldered (col 9, lines 35-38)

Regarding claims 8-9, 14, and 51-52, Lake et al disclose that the conducting material is copper foil.

Regarding claims 10 and 12, Lake et al disclose that the conducting material may be electroplated (col 9, line 57).

Regarding claim 13, Lake et al disclose the dielectric material of a first structure is bonded to the conducting material of a second structure.

Regarding claim 15, Lake et al disclose that the dielectric material is applied to the foil using a press roll (col 9, line 15).

Regarding claims 16 and 45, Lake et al disclose that the conducting material is patterned with a resist, which is a protective cover.

Regarding claim 17, Lake et al disclose that the passages may be formed by plasma etching or by laser (col 8, lines 16-17).

Regarding claim 18, see alternate embodiment in Figure 1 of Lake et al, wherein the conducting material deposited in a passage does not extend beyond the opening of the passage.

Regarding claim 19, see Figure 8, step 5, or Lake et al.

Regarding claims 20-21, and 53, Lake et al disclose that the conducting material is a metal deposited in the passages in by platting (col 9, line 6).

Regarding claims 24-26, 28, 29, 30, 31, 33, 54, 55, and 56, Lake et al disclose a layer of tin lead alloy may be applied over the copper foil by a continuous electroplating process (col 9, lines 57-59).

Regarding claim 32, Lake et al disclose that the circuitry is formed by resist patterning (col 8, lines 55-58).

Regarding Claims 36 and 63, Lake et al disclose that the layers will be soldered coated (col 9, line 39).

Regarding claims 42, 64, and 65, Lake et al disclose that the structures are filled with a thermoset plastic.

7. Claims 1, 37-42, 46, 66, 67, and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by GB 2203290 to Hamilton.

Regarding claims 1, 46, 66, 67, and 68, Hamilton discloses a multi-layered electronic structure and a method for making said structure (see Figure 8), comprising the steps of:

a. providing a layer of dielectric material (12) having a top and bottom;

b. providing a layer of electrically conducting material (11,13) on one of the top surface and the bottom surface of the dielectric layer;

c. forming at least one passage (14) through the dielectric layer;

d. depositing electrically conducting material (15) in at least one of the at least one passage through the dielectric layer;

e. removing portions of the layer of electrically conducting material to define a pattern of circuitry (see Figure 6);

f. stacking a plurality of structures (see Figure 7) comprising the layer of dielectric material and layer of electrically conducting material;

g. aligning the plurality of structures (it is inherent that the structures are aligned);

h. joining the plurality of structures such that the electrically conducting material in at least one on the at least one passage through the dielectric material electrically connects the conductive pattern disposed on the dielectric layer with another conductive pattern on an adjacent structure of the stacked plurality of structures (by bonding, page 3, lines 32+); and

i. filling the spaces between the structures with electrically insulating material.

Regarding claims 37-42, see pages 3-4, lines 32+ of Hamilton, regarding bonding via pressure in a vacuum under inert atmosphere.

8. Claims 1, 46, 66, 67, and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by either US Patent 3,311,966 to Shaheen et al, US Patent 3,464,855 to Shaheen et al, US Patent 5,707,749 to Katagiri et al, US Patent 4,353,957 to Rutt et al, or US Patent 5,481,795 to Hatakeyama et al.

Applicant is referred to figures and disclosures in each for specifics.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4, 11, 27, 35, 49, 57, 58, and 60-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lake et al.

Lake et al disclose the invention cited above. However, they do not disclose the particulars of the invention as claimed by Applicant.

Regarding claims 27 and 57, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provide a cap having a thickness of 0.0001 to .0004 inch, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claims 35, 60-62, Official Notice is taken that aligning structure such as providing holes in the laminate layers and a jig having corresponding aligning pins and indicia (registration marks) are well known in the art. Applicant, also alludes to the fact such structures are known, referring to slots and pins as standard alignment means (page 34, lines 2-3).

Regarding claims 4 and 49, Official Notice is taken that liquid crystal polymer film is well known in the circuit board arts and a skilled artisan would have found it obvious at time of invention to use such in the method of Lake et al.

Regarding claim 11, Official Notice is taken that applying a coating by physical vapor deposition to a substrate comprising vacuum evaporation or sputtering is well known in the art and a skilled artisan would have found it obvious at time of invention to use such in the method of Lake et al.

Regarding claim 58, Official Notice is taken that coating a substrate with oxides (e.g. tin oxide) are known in the art to roughen the surface for subsequent bonding and a skilled artisan would have found it obvious at time of invention to apply a coating for such purpose.

11. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lake et al in view of US Patent 3,601,523 to Arndt.

Lake et al disclose the invention cited above. However, they do not disclose that the conducting material provided in the passage is a conducting paste.

Arndt discloses a method for filling a passageway with a conducting paste in order to conductively contact the circuitry from one side of a dielectric to another. .

Regarding claim 22, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a conducting paste in the passage of Lake et al, in light of the teachings of Arndt, in order to provide a more low resistant connection than by platting (see col 1, lines 60+).

Regarding claim 23, Arndt uses a squeegee (20) to apply the conducting paste.

12. Claims 34 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lake et al in view of US Patent 4,921,157 to Dishon et al.

Lake et al disclose the invention cited above. However, they do not disclose treating the dielectric layer and patterned circuitry with fluorine-containing plasma.

Dishon et al disclose a method for treating a circuit board with exposed soldering. The surfaces are treated with a fluorine-containing plasma in order to remove oxides and provide a more efficient solder joint.

Regarding claims 34 and 59, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have treated the structure of Lake et al with fluorine-containing plasma, in light of the teachings of Dishon et al, in order to remove surface oxides from the solder contacts.

13. Claims 37-44 and 69-78 rejected under 35 U.S.C. 103(a) as being unpatentable over either Lake et al or Hamilton in view of US Patent 5,635,010 to Pepe et al.

Lake et al and Hamilton disclose the invention cited above. Both, reference rely on pressure and heat to bond the structures. However, neither specifically discloses providing filling the spacing between adjacent structures with a liquid, which is transformed into a solid.

Pepe et al disclose a method for bonding layers to form a laminate (see Figures 9-12). A dielectric adhesive, preferably a polyimide, applied as a liquid is provide on the to close voids and help bond substrates together. "The preferred polyimide exhibits sufficient viscous flow at the initial temperature and pressure conditions such that it fills all voids between adjacent chips and excess adhesive extrudes from the chip stack to achieve minimal thickness of the adhesive layer" (col 7, lines 58-63).

Regarding claims 37 and 69, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided a liquid insulator to bond the structures of Lake et al, in light of the teachings of Pepe et al, in order to fill the voids between the structures.

Regarding claims 37-44, and 76-78, see col 8, lines 49-64 of Pepe et al regarding bonding with pressure in a vacuum with an inert atmosphere.

Regarding claims 70-71, the liquid may include epoxy, an organic resin.

Regarding claims 73-74, Official Notice is taken that inorganic filler and cross-linking is the art to provide structures of added strength and that a skilled artisan would have found it obvious at the time of invention to have provided either for such purpose.

Regarding claim 74, it is inherent that the liquid resin is moved by capillary action.

Regarding claim 75, the liquid resin is placed on the top periphery of the structures.

Prior Art References

The prior art references listed on the enclosed PTO-892, but not used in a rejection of the claims, are cited for their teachings of teachings of forming a multi-layered electronic structure.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Compton whose telephone number is (703) 305-0240. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory M. Vidovich can be reached on (703) 308-1513. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9302 for regular communications and (703) 872-9303 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1148.

GREGORY M. VIDOVICH
PRIMARY EXAMINER

ebc E.C
September 5, 2002